

**SUBJECT:**

**Digital Electronics**

**Part-I**

Q1 Answer the following questions: (2 x 10)

- a) Find the hexadecimal number of  $(243)_8$ .
- b) Explain the role of transistors as switches in digital circuits.
- c) How many OR gate and half adder are required to implement a full adder Circuit?
- d) What is race around condition?
- e) What is essential prime implicant?
- f) What is the difference between combinational circuit and Sequential circuit?
- g) Design NAND gate and XOR gate using 2 - input NOR gate.
- h) What is a hazard in a combinational circuit?
- i) Convert the 100110 binary code into gray code.
- j) A 4 bit modulo-16 ripple counter uses JK flipflops. If the propagation delay of each Flipflop is 50 ns. Then find the maximum clock frequency.

**Part-II**

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- a) If  $X = 111.101$  and  $Y = 101.110$ , Calculate  $X + Y$ ,  $X - Y$ , and  $Y - X$  by using 2's Complement method.
- b) Use the K-Map to simplify the expression  $\_ = \_ . \_ + \_ \_ B$ .
- c) Implement the function  $= \_ + \_ + \_$  using NAND gate only.
- d) Use the Quine-McCluskey technique to minimize the following Boolean function:  $\_ , \_ = \sum 1, 3, 5, 7$
- e) Write short note on Mealey Morre Model of Finite State Machine.
- f) Design of NAND gate using CMOS.
- g) Explain the different types of Laws in Boolean function.
- h) Define and explain the operation of 4 bit shift register?

i) Design a 3-bit binary counter using T flip flop.

j) Design a Full adder circuit.

k) Differentiate between decoder and demultiplexer. Under what circumstance a decoder can be converted into demultiplexer?

l) Design and explain the Johnson Counter.

### **Part-III**

Only Long Answer Type Questions (Answer Any Two out of Four)

(6+10)

Q3 a) Design of  $8 \times 1$  MUX using  $2 \times 1$  MUX. b) Given that f

A, B, C, D =  $\sum 0, 1, 5, 7, 10, 14, 15$ . Implement this function using an appropriate Multiplexer.

Q4 a) Derive the Characteristic Equation of D Flipflop.

(6+10)

b) Convert the SR Flipflop to JK Flipflop.

Q5 a) Minimize the Four variable logic function using K-Map. f A, B, C, D =  $\sum$  \_

0, 1, 2, 3, 5, 7, 8, 9, 11,14\_  
(8+8)

b) Design a simple logic circuit such that the outputs is 1 when the binary number A, B, C, D is greater than 0110.

Q6 a) What are the salient features of an Algorithmic State Machine (ASM) chart? (6+10)

b) Design an ASM chart for a simple weighing machine.